REMARKS

Claims remaining in the present patent application are Claims 1-23.

Claims 1, 10, and 15 are amended herein. No new matter is added as a result of the Claim amendments. Please cancel Claims 3 and 19.

35 U.S.C. § 112

Claims 1-23 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant continues to respectfully assert that the rejections of Claims 1-7 and 9-23 reflect an improper application of 35 U.S.C. § 112, second paragraph. Applicant respectfully asserts that claims are not required to specify every element required for enablement if such is well known. Applicant respectfully asserts that one of ordinary skill in the art would understand Claims 1-23 to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

For example, the Applicant respectfully submits that one skilled in the art would typically interpret Claim 1 to mean that the delay lock loop mode is associated with the first feedback loop, and that the phase locked loop mode is associated with the second feedback loop.

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With respect to Claim 1, the rejection continues to state, "it is unclear when 'in a delay lock loop mode and a phase locked loop mode' will be happened [sic] and how the phase detector and the phase frequency detector can recognize the modes." Applicant again respectfully asserts that the claim limitations are read in light of the descriptions of the specification and that claims are not required to specify every technical detail required for enablement. The Applicant respectfully submits that an explanation of how the modes are recognized are explained in detail in the specification with reference to step 730 of Figure 7 (page 19, line 4 - page 20, line 14). Accordingly, the Applicant respectfully asserts that one of ordinary skill in the art could distinctly identify the subject matter of Claim 1 which the Applicant regards as the invention.

With reference to Claim 3, the rejection states that it is unclear how the modes can be switched since no means for performing the switching function is recited. The Applicant respectfully asserts that one of ordinary skill in the art would understand that some means for performing the switching function would be inherent in the claim limitation recited in Claim 3. Applicant again respectfully asserts that the technical description of the invention of these details is the proper purview of the specification and that claims are not required to specify every detail required for enablement. Accordingly, the

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Applicant respectfully asserts that one of ordinary skill in the art could distinctly identify the subject matter of Claim 3 which the Applicant regards as the invention.

With respect to Claim 10, the rejection continues to state, "it is not understood how the delay blocks can be "configured" as recited on line 4 and how the generator can be "operated" as a voltage controlled oscillator on line 7 and what the "coarse adjustment" and "fine adjustment" are and how these adjustments can be performed. Furthermore, the Applicant respectfully asserts that one of ordinary skill in the art would understand the recited limitation of configuring a plurality of dynamically controlled delay blocks as a voltage controlled delay line. The Applicant further asserts that one of ordinary skill in the art would understand the recited limitation of operating a voltage controlled oscillator in a phase locked loop mode. The Applicant again respectfully asserts that answering the technical details regarding how the generator is operated and how the delay blocks can be configured are the proper purview of the specification and that the claims are not required to specify every element required for enablement.

With reference still to Claim 10, the rejection states that it is not understood what the "coarse adjustment" and the "fine adjustment" are and

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how these adjustments can be performed. The Applicant respectfully asserts that one of ordinary skill in the art could clearly understand the terms "coarse adjustment" and "fine adjustment." Furthermore, one of ordinary skill in the art would understand that a coarse adjustment is inherently performed prior to performing a fine adjustment. The Applicant further asserts that the question of how these adjustments can be performed is the proper purview of the specification and that there in no requirement that Claim 10 specifies how these are performed. Accordingly, the Applicant respectfully asserts that one of ordinary skill in the art could distinctly identify the subject matter of Claim 10 which the Applicant regards as the invention.

With reference to Claim 15, the rejection continues to state, "it is not understood how the phase generator can be "configurable" in a first mode and a second mode and how the generator can be coupled to the detectors since no means for performing the coupling function is recited and the generator cannot perform the coupling function. The Applicant again asserts that one of ordinary skill in the art would understand a circuit having a phase generator that is coupled with phase detector in a delay lock loop as recited in Claim 15.

Furthermore, the Applicant asserts that one of ordinary skill in the art would understand a circuit having a phase generator that is coupled with a phase-frequency detector in a phase locked loop as recited in Claim 15. Furthermore,

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one skilled in the art would clearly understand either of those circuits whether or not an input/output was specifically recited. Additionally, one of ordinary skill in the art would clearly understand that the phase generator itself is not performing the coupling function. Accordingly, the Applicant respectfully asserts that one skilled in the art could distinctly identify the subject matter of Claim 15 which the Applicant regards as the invention.

With reference to Claim 16, the rejection states that, "the description of the present invention is incomplete because the phase detector is not connected to anything. Thus, the claimed detector may not perform the recited function. The Applicant respectfully asserts that Claim 15 clearly recites that the phase detector is coupled with the phase generator in a delay lock loop. The Applicant further asserts that one of ordinary skill in the art would understand the claim limitation of a phase detector in a delay lock loop comparing an input signal with a signal received via a first feedback line as recited in Claim 16 of the present invention. Accordingly, the Applicant respectfully asserts that one skilled in the art could distinctly identify the subject matter of Claim 16 which the Applicant regards as the invention.

With reference to Claim 19, the rejection states, "it is unclear how the control signal can change the first mode and the second mode since the phase

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detector is not connected to anything." Again, the Applicant respectfully asserts that Claim 15 recites a phase generator configurable in a first mode wherein the phase generator is coupled with a phase detector in a delay lock loop. The Applicant respectfully asserts that Claim 15 also clearly recites that the phase generator is configurable in a second mode when a phase-frequency detector is coupled with the phase generator in a phase locked loop. The Applicant respectfully asserts that one of ordinary skill in the art would clearly understand the claim limitation wherein the phase detector generates a second control signal for changing between the first mode and the second mode as recited in Claim 19 of the present invention. Accordingly, the Applicant respectfully asserts that one skilled in the art could distinctly identify the subject matter of Claim 19 which the Applicant regards as the invention.

With reference to Claim 20, the rejection states that, "the description of the present invention is incomplete because the phase detector is not connected to anything. Thus, the claimed detector may not perform the recited function. The Applicant respectfully asserts that Claim 15 clearly recites that the phase-frequency detector is coupled with the phase generator in a phase locked loop. The Applicant further asserts that one of ordinary skill in the art would understand the claim limitation of a phase-frequency detector in a phase locked loop comparing an input signal with a signal received from the phase generator

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via a second feedback line as recited in Claim 20 of the present invention.

Accordingly, the Applicant respectfully asserts that one skilled in the art could distinctly identify the subject matter of Claim 20 which the Applicant regards as the invention.

35 U.S.C. § 102

Claim 10 stands rejected under 35 USC § 102(b) as allegedly anticipated by Kurd (US 6,043,717, "Kurd"). Applicant has carefully reviewed the cited reference and respectfully asserts that embodiments of the present invention as recited in Claim 10 are not anticipated or rendered obvious by Kurd. Claim 10 of the present invention recites (emphasis added);

A method for generating multiple phases of an input signal comprising:

a phase generator accessing said input signal, said phase generator comprising a plurality of dynamically controlled delay blocks;

configuring said plurality of dynamically controlled delay blocks as a voltage controlled delay line in an delay lock loop mode to perform coarse adjustment;

generating a signal by a phase detector to cause said phase generator to operate in a phase locked loop mode; and

operating said phase generator as a voltage controlled oscillator in said phase locked loop mode for fine adjustment.

Applicant respectfully asserts that Kurd does not teach or suggest generating a signal by a phase detector to cause a phase generator to operate in a phase locked loop mode as recited by Claim 10. In contrast, Kurd teaches a selection of the operating mode of the circuit is via a mode select input 255

CYPR-CD02216 Serial No.: 10/774,180 Examiner: Le, D. T. 14 Group Art Unit: 2816 which is separate from the phase detector. Accordingly, the Applicant respectfully asserts that the rejection of Claim 10 of the present invention overcome under 35 U.S.C. § 102(b) is overcome.

35 U.S.C. § 103

Claims 1-5, 8-17 and 19-23 stand rejected under 35 USC § 103(a) as allegedly unpatentable over Dunn (US 4,069,462, "Dunn") in view of Kurd (US 6,043,717, "Kurd"). Applicant has carefully reviewed the cited references and respectfully asserts that embodiments of the present invention as recited in Claims 1-5, 8-17 and 19-23 are not rendered obvious by Dunn in view of Kurd.

Claims 1-5, 8-17 and 19-23 recite, in part, a delay lock loop circuit or mode. Applicant respectfully asserts that Dunn actually <u>teaches away</u> from a delay lock loop circuit or mode as claimed by teaching using "only phase synchronization so that the phase lock-up time is predictable..." (column 2, lines 38-39). Furthermore, Dunn does not teach or suggest replacing VCO 17 with a device which is capable of operating in a delay lock loop mode or in a phase locked loop mode as recited in Claims 1-5, 8-17 and 19-23 of the present invention. Thus, it would be counter-intuitive, based upon the teaching of Dunn, to utilize a device capable of operating in a delay lock loop mode or in a phase locked loop mode.

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Furthermore, the Applicants respectfully submit that the determination of obviousness cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the present invention absent a suggestion for the combination in the claimed fashion. There must be a teaching or suggestion within the prior art to select particular elements, and to combine them in the way claimed. The Applicants respectfully submit that Dunn fails to teach or suggest a device which is capable of operating in a delay lock loop mode or in a phase locked loop mode, but instead teaches away from the recited claim limitations by teaching the use of phase synchronization only in order to make phase lock up time more predictable.

Further, Applicants respectfully assert that the proposed modification of Dunn in view of Kurd does not teach or suggest first and second output signals of a phase generator as recited by Claim 1. In contrast, both Dunn and Kurd show a single output.

As described above, Kurd fails to teach or suggest that a signal from a phase detector causes the phase generator to operate in either a delay lock loop mode or phase locked loop mode as recited in Claims 1, 10, and 15 of the present invention. Furthermore, Dunn fails to overcome the shortcoming of Kurd. More

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specifically, Dunn fails to teach or suggest that a signal from a phase detector causes the phase generator to operate in either a delay lock loop mode or phase locked loop mode as recited in Claims 1, 10, and 15 of the present invention.

Accordingly, the Applicant respectfully asserts that the rejection of Claims 1, 10, and 15 of the present invention, as well as dependent Claims 2, 4-9, 11-18, and 20-23, overcome under 35 U.S.C. § 103(a) are overcome.

Claims 6-7 and 18 stand rejected under 35 USC § 103(a) as allegedly unpatentable over Dunn (US 4,069,462, "Dunn") in view of Kurd (US 6,043,717, "Kurd") and further in view of Paakinson (JP404227314A, "Paakinson").

Applicant has carefully reviewed the cited references and respectfully asserts that embodiments of the present invention as recited in Claims 6-7 and 18 depend from allowable base claims. More specifically, Kurd alone, or in combination with Dunn, does not teach or suggest that a signal from a phase detector causes the phase generator to operate in either a delay lock loop mode or phase locked loop mode as recited in Claims 1, and 15 of the present invention. The Applicant respectfully asserts that Paakinson similarly fails to teach or suggest that a signal from a phase detector causes the phase generator to operate in either a delay lock loop mode as recited in Claims 1 and 15 of the present invention. Accordingly, the Applicant

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respectfully asserts that the rejection of respectively dependent Claims 6-7 and 18 under 35 U.S.C. § 103(a) are overcome.

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CONCLUSION

Claims remaining in the present patent application are Claims 1-2, 4-18, and 20-23. The Applicants respectfully request consideration of the above captioned patent application in light of the remarks presented herein.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

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